Evolutionary Recovery of Electronic Circuits from Radiation Induced Faults

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***Abstract*—Radiation Hard technologies for electronics are the conventional approach for survivability in high radiation environments. This paper presents a novel approach based on Evolvable Hardware. The key idea is to reconfigure a programmable device, in-situ, to compensate, or bypass its degraded or damaged components. The paper demonstrates the approach using a JPL-developed reconfigurable device, a Field Programmable Transistor Array (FPTA), which shows recovery from radiation damage when reconfigured under the control of Evolutionary Algorithms. Experiments with total radiation dose up to 350kRad show that while the functionality of a variety of circuits, including a rectifier and a Digital to Analog Converter implemented on a FPTA-2 chip, is degraded/lost at levels before 100kRad, the correct functionality can be recovered through the proposed evolutionary approach. The Evolutionary Algorithm controls the state of about 1,500 switches that determine configurations on the FPTA-2 programmable device. Evolution is able to use the resources of the reconfigurable cells, even radiation damaged components, to synthesize a new solution.**

I. Introduction

Long-life space missions and extreme environments have characteristics such as high radiation level (Europa Surface and Subsurface mission, 5 MRad), high temperature (Venus Surface Exploration and Sample Return mission, 460°C) and low temperature (Titan in-situ mission, -180°C). Such missions and environments have dictated the need for new electronics technologies.

Electrons and protons in space can cause permanent damage in electronic devices that can lead to operational failure. Particularly, Single Event Effects (SEE) are radiation induced errors in microelectronic circuits caused when charged particles lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs. These events can be either transient and non-destructive (Single Event Upset) or hard and potentially destructive events (Single Event Latchup).

One technique for environments with high levels of radiation is the use of Radiation Hard technologies such as Silicon on Insulator (SOI), which allows compensating for the effect of radiation. However, the fabrication cost associated with extreme environment electronics is high. In this paper we will present another technique, based on Evolvable Hardware, for electronic survivability in high radiation environments.

A reconfigurable chip developed at JPL, the Field Programmable Transistor Array (FPTA-2) chip, is used in the experiment described in this paper. We submitted this chip to radiation using JPL facilities, applying a total dose ranging up from 10kRads up to 75kRads at a time and a cumulative dose up to 350kRads. These parts are not radiation hardened. When the chip was back from the radiation chamber, the permanent radiation induced faults (single event latch-up) caused a deterioration in the behavior of some circuits (D/As, filters, rectifiers) previously downloaded/programmed onto the chip. We show that the correct functionality of these circuits can be recovered using Evolutionary Algorithms. The Evolutionary Algorithms control the state of about 1,500 switches. Using a population of about 500 candidates and after running the Evolutionary process for about 200 generations, the correct functionality is recovered. Evolution is able to use the resources of the reconfigurable cells, even the radiation damaged components, to synthesize a new solution.

The results indicate that using Evolvable Hardware technology we can design and develop electronic components and systems that are inherently insensitive to radiation induced faults by using on-board evolution in hardware to achieve fault-tolerant and highly reliable systems. The long term results of the proposed research would allow electronics to adapt to an extreme environment and long mission duration.

A number of researchers in the literature have examined the effect of radiation on CMOS devices [1,2]. These could be classified into those researchers who studied the effect

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of radiation on various cells and macro-blocks fabricated in silicon [3-9] or those who considered the design of radiation hardened components and cell libraries [10-14]. Works on studying the impact of radiation have considered custom implementation and conventional digital FPGA platforms such as Xilinx [15-19]. These works have been focusing on studying both total dose radiation effects, where the effect is permanent, and Single Event Upsets (SEUs), where individual bits in memory elements flip when exposed to certain quantity of radiation.

However, most of these researchers seem to have focused on technologies which are above 0.5 micron and hence the effects could not be generalized to devices implemented in the latest Deep Sub Micron (DSM) technologies, where leakage currents dominate. In addition, no research has been carried out on the development of custom reconfigurable architectures implemented at transistor level hence enabling the implementation of both analogue and digital circuits.

This paper presents a framework for the development of radiation tolerant mixed analogue and digital circuits on a DSM reconfigurable CMOS device. Experiments are carried out in which the device is subjected to various radiation dosages, using an X-ray based radiation source, and the performance of the device is tested by mapping a number of functional circuits. When the device fails any of the tests, an evolutionary algorithm is used to recover the functionality of the device where possible.

The rest of this paper is structured as follows: Section 2 describes the Field Programmable Transistor Array (FPTA) device architecture. Section 3 describes the procedure followed during radiation tests. Section 4 describes the overall system architecture which includes the data acquisition system. Section 5 provides an analysis of results obtained. Finally, the main conclusions of the work are listed in section 6.

II. FPTA Architecture

The FPTA is an evolution-oriented reconfigurable architecture (EORA). Important characteristics needed by evolution-oriented devices are *total accessibility*, needed in order to provide evolutionary algorithms the flexibility of testing in hardware any chromosomal arrangements, some of which may be dangerous for existing commercial devices (may lead to internal bus allocation conflicts and burn the chip) and thus forbidden, *granularity at low level* (here transistor) allowing evolution to choose/construct the most suitable building block for certain system, and *transparency*, which enables users to have access to internal device information, etc.

The FPTA has a configurable granularity at the transistor level. It can map analog, digital and mixed signal circuits. The architecture is cellular, with each cell having a set of transistors, which can be interconnected by other "configuration transistors". For brevity, the "configuration transistors" are called switches. However, unlike conventional switches, these can be controlled for partial opening, with appropriate voltage control on the gates, thus allowing for transistor-resistor type topologies.

The architecture of the FPTA consists of an 8x8 array of re-configurable cells. Each cell has a transistor array as well as a set of programmable resources, including programmable resistors and static capacitors. Figure 1 provides a broad view of the chip architecture together with a detailed view of the reconfigurable transistor array cell. The re-configurable circuitry consists of 14 transistors connected through 44 switches. The re-configurable circuitry is able to implement different building blocks for analog processing, such as two and three stages OpAmps, logarithmic photo detectors, or Gaussian computational circuits. It includes three capacitors, Cm1, Cm2 and Cc, of

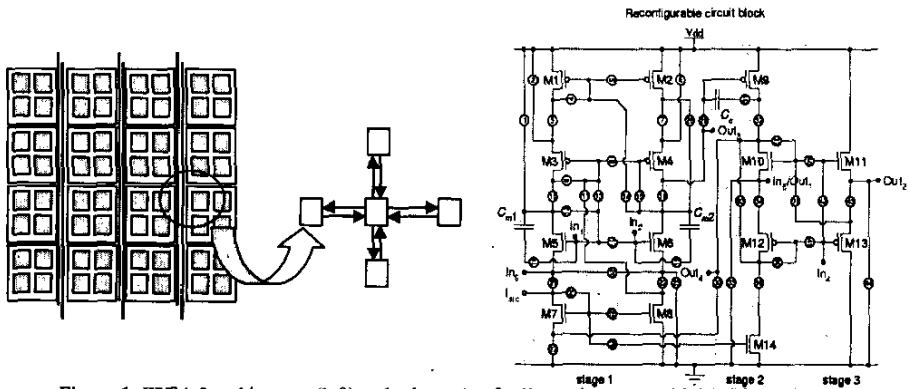


Figure 1: FPTA 2 architecture (left) and schematic of cell transistor array (right). The cell contains additional capacitors and programmable resistors (not shown).

100fF, 100fF and 5pF respectively. Control signals come on the 9-bit address bus and 16-bit data bus, and access each individual cell providing the addressing mechanism for downloading the bit-string configuration of each cell. A total of ~5000 bits is used to program the whole chip. The pattern of interconnection between cells is similar to the one used in commercial FPGAs: each cell interconnects with its north, south, east and west neighbors. This is the first mixed-signal programmable array, FPMA, in the sense that its cells can be configured as both analog and digital circuitry; with its 64 cells it can configure more Operational Amplifiers (OpAmps) than the largest commercial Field Programmable Analog Array (FPAA) chip (which contains only 20 OpAmps) [21].

III. Experimental Procedure

The radiation source used was an electron beam obtained from a dynamitron accelerator. The electrons are accelerated at an energy of 1 MeV in a small vacuum chamber with a beam of 8". The fluxes in the small chamber was 4.E9 [e/(s.cm2)] which is around 300 rad/sec.

The procedure for exposure to radiation, test, and recovery was as follows; 4 different samples of the FPTA chip were exposed to radiation at a time. Two of the samples were under electronic bias, i.e, with power on (chip B1 and chip B2), whereas, the other two remained un-biased, i.e., with power off (chip U1 and chip U2). Due to space limitations in the chamber, only two chips could be radiated at a given time, so the biased and un-biased sets were alternated under the same radiation dose.

Both the biased and un-biased sets were exposed to radiation doses ranging from 0 to 350Krad at 50Krad steps. Figure 2 illustrates the incremental radiation profile to which the chips were subjected to over a period of 7 days.

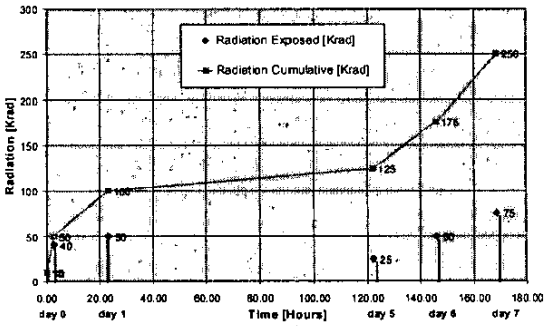


Figure 2: Cumulative radiation and experimental schedule.

After each radiation step both biased and un-biased sets were tested by downloading the configuration for the following tests/circuits respectively: Identity test, rectifier circuit, Tunable filter and 4-bit D/A converter circuit.

The identity test is specially designed to test the switching elements, i.e. transmission gates, within the FPTA. It operates by propagating a sinusoidal signal to the output through exercising the correct set of transmission gates within the FPTA. The rectifier, tunable filter, and the 4-bit D/A converter are examples of relatively large macro blocks of the FPTA which are utilized within sensor interfacing circuitry. The identity circuit is evolved using only one FPTA cell. The half-wave rectifier uses four cells; the tunable filter uses 10 cells and the DAC uses 20 cells. The tunable filter is evolved to amplify a 1kHz tone and attenuate a 10kHz tone applied at the circuit input.

IV. System Architecture

A complete stand-alone board-level evolvable system (SABLES) is built by integrating the FPTA and a DSP implementing the Evolutionary recovery algorithm, as shown in Figure 3. The system is connected to the PC only for the purpose of receiving specifications and communicating back the result of evolution for analysis. The system fits in a box 8" x 8" x 3". Communication between DSP and FPTA is very fast with a 32-bit bus operating at 7.5MHz. The FPTA can be attached to a Zif socket attached to a metal electronics board to perform extreme temperature and radiation experiments The evaluation time depends on the tests performed on the circuit. Many of the tests attempted here require less than two milliseconds per individual, and runs of populations of 100 individuals from 100 to 200 generations require only 20 seconds.

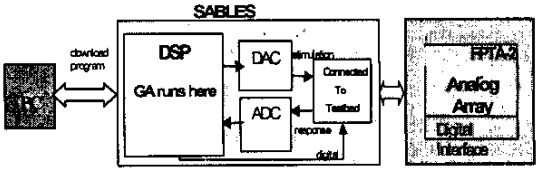


Figure 3: Complete System Architecture.

V. Results

Tables 1-4 illustrate results of radiation tests for dosages of 100Krad, 175Krad, 250Krad, and 350Krad respectively. Each table illustrates the experimental results with the various tests described in section 3 using both biased and un-biased test chip samples. There are two circuits in each test, a reference and a recovery. The reference circuit is either designed by humans or was obtained by evolution previous to radiation. The recovery circuit was obtained after applying evolution to the chip after radiation. The (grey) shaded cells highlight a successful recovery through evolution. The white cells in the table indicate either of two cases: a failure of the specific test with the

corresponding chip (recovery failed); or that the reference circuit was not affected by the radiation. For each test any noticeable change in the behavior of input/output signals are reported. For example in table 1, U2 sample initially suffers a 50% drop in amplitude after reaching an accumulative dosage of 100krad (Half-wave rectifier). This is later recovered through evolution in 311 generations.

After a total dose of 100Krad a number of sample chips suffered from some distortion in the shape of the output waveform. This is mainly observed as a drop in amplitude of the signal. When evolutionary recovery is triggered most of these distortions are overcome and the true functionality is obtained. It could be noted from the table 1 that the un-biased chip U1 starts to malfunction at 100Krad with most tests failing drastically such that recovery is not possible.

As the radiation dosage is increased to 175 Krad, the distortion on the output increases for the half-wave rectifier. For example, the rectifier for both B1 and B2 passes the input unchanged. However, in almost all cases the evolutionary recovery system is able to correct the output to the required shape. Figure 4(a) illustrates the response of the rectifier at 50krad on the sample B1 chip. After exposure to radiation of up to 175Krad the rectifier malfunctions as the output response is identical to that of the input shown on Figure 4(b). When the evolutionary mechanism is activated, the correct output response is retained as shown in Figure 4(c).

It can be observed from Tables 1 and 2 that, in most cases, the chip seems to be more damaged at 100krad than at 175krad, particularly for U1. The literature also reports [1] a phenomenon in which more damage occurs at low dose rates compared to the damage that is observed at high dose rates. This effect is called enhanced degradation at low dose rate.

TABLE 1: Experimental results at 100kRads on chip samples un-bias U1, U2 and bias B1 and B2. (In the case of the tunable filter G represents the gain/attenuation at 1kHz and 10kHz).

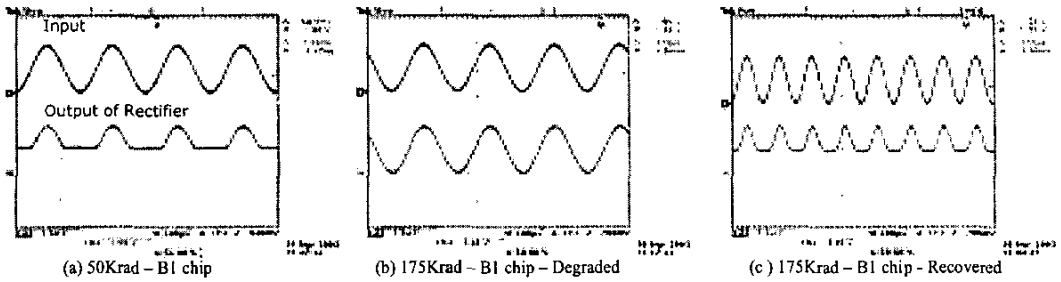
U1		U2		B1		B2	
Reference	Recovery	Reference	Recovery	Reference	Recovery	Reference	Recovery
IDENTITY							
Flat Response	Flat response for all chromosomes	Correct		Correct		Shape output distorted	Recovered - Sine wave slightly clipped on the rising edge
HALF-WAVE RECTIFIER							
Flat response	Flat response for all chromosomes	Amplitude drops 50%	Recovered Gen = 311	Amplitude drops 50%	Recovered Gen = 300	Low Amplit. Sine wave	Recovered Gen=242
TUNABLE (LOW-PASS) FILTER							
Flat Response (f=1kHz, G= -55dB) (f=10kHz, G=-50dB)		Correct Response (f=1kHz, G= -1dB) (f=10kHz, G=-12dB)		Correct Response (f=1kHz, G= 0dB) (f=10kHz, G=-12dB)		Low gain at 1kHz (f=1kHz, G= -24dB) (f=10kHz, G=-45dB)	Recovered Response (f=1kHz, G=2dB) (f=10kHz, G=-14dB)
4 BIT DAC							
Failed	Failed	Correct		Correct		Failed	Recovered at generation 200

TABLE 2: Experimental results at 175 kRads.

U1		U2		B1		B2	
Reference	Recovery	Reference	Recovery	Reference	Recovery	Reference	Recovery
IDENTITY							
Correct		Correct		Correct		Correct	
HALF-WAVE RECTIFIER							
The shape has been changed. No rectification.	Recovered after 901 generations	Correct		The input is observed at the output	Recovered After 677 generations	The input waveform is observed at the output	Recovered after 200 generations
TUNABLE (LOW-PASS) FILTER							
Correct Response (f=1kHz, G= -2dB) (f=10kHz, G=-17dB)		Correct Response (f=1kHz, G= -3dB) (f=10kHz, G=-18dB)		Correct Response (f=1kHz, G= -2dB) (f=10kHz, G=-15dB)		Low gain at 1kHz (f=1kHz, G= -10dB) (f=10kHz, G=-25dB)	Recovered Response (f=1kHz, G= -1dB) (f=10kHz, G=-11dB)
4 BIT DAC							
Failed	Recovered a 3-bit DAC	Correct		Failed	Recovered with lower voltage range and small glitch for bit 4	Failed	Recovered with lower voltage range

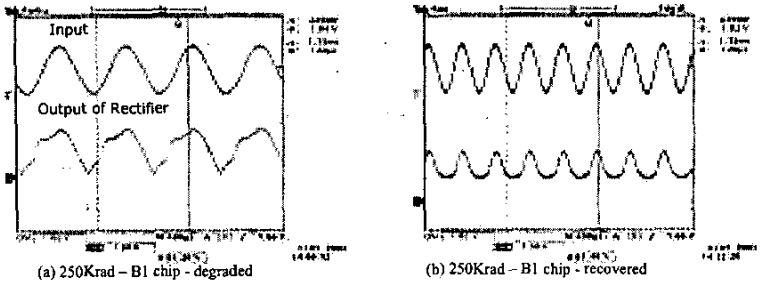
As the dosage is increased to 250Krad (Table 3), cases appear where the evolutionary algorithm is unable to recover the correct functionality on the output (discarding U1 due to its inconsistent behavior). However, in most cases recovery is achieved. Again considering the rectifier circuit at 250krad as illustrated in Figure 5(a), the output response is clearly distorted due to radiation. However, the correct output response is recovered once the evolutionary mechanism takes over, even though the final circuit suffers from some non-ideal behavior when the output is low.

As the dosage reaches 350 Krad (Table 4), there is a clear failure pattern with all tests, with the evolutionary algorithm unable to recover any of the required functionality.



(a) 50Krad – B1 chip (b) 175Krad – B1 chip – Degraded (c) 175Krad – B1 chip - Recovered

Figure 4: Response of the Rectifier circuit at (a) 50kRads, (b) after being radiated to 175kRads resulting in deterioration through loss of rectification, followed by (c) recovery through Evolution.



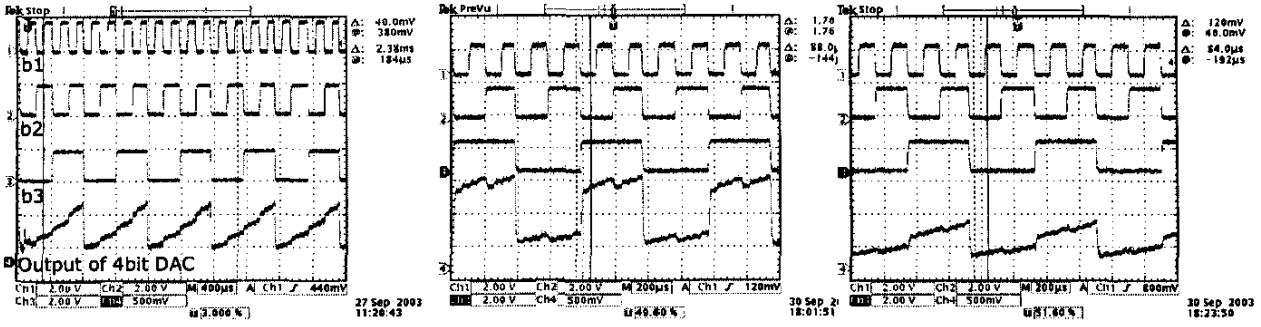
(a) 250Krad – B1 chip - degraded (b) 250Krad – B1 chip - recovered

Figure 5: Response of the Rectifier circuit at (a) 250kRads resulting in distortion, followed by (b) recovery through Evolution

TABLE 3: Results with 250kRads

U1		U2		B1		B2	
Reference	Recovery	Reference	Recovery	Reference	Recovery	Reference	Recovery
IDENTITY							
Flat Response	Flat response for all chromosomes	Correct		Slight Deterioration at the output	Recovered with slight decrease in the voltage level	Output equal to 0	Perfect waveform recovered
HALF-WAVE RECTIFIER							
Flat response	Recovery failed	Correct		Output follows the input with distortion	Recovered after 1337 generations	Output follows the input with attenuation	Recovered After 79 generations
TUNABLE (LOW-PASS) FILTER							
Flat Response (f=1kHz, G= -25dB) (f=10kHz, G=-24dB)	Recovery failed	Correct Response (f=1kHz, G= -3dB) (f=10kHz, G=-18dB)		Flat Response (f=1kHz, G=-30dB) (f=10kHz, G=-27dB)	Recovery failed	Low gain at 1kHz (f=1kHz, G= -10dB) (f=10kHz, G=-25dB)	Recovered Response (f=1kHz, G= -4dB) (f=10kHz, G=-18dB)
4 BIT DAC							
Output follows bit 4	Flat output	Correct		Output follows bit 4	Partial recovery: Monotonic wave was obtained but the amplitude is dropped to half.	Non-monotonic output	Recovered failed

Figure 6 demonstrates another example of recovery through evolution using the example of the 4-bit DAC circuit. Figure 6(a) illustrates a correct functioning DAC at 100Krad. When radiation dosage is increased to 175Krad, the circuit malfunctions with clear loss in discrimination between various input values. This is associated with a loss in the monotonic nature of the response, see Figure 6(b). When evolution is activated the response is recovered, however, as could be seen from Figure 6(c) there is some deterioration in the signal level.



(a) 100Krad – B1 chip (b) 175Krad – B1 chip - degraded (c) 175Krad – B1 chip - recovered

Figure 6: Response of a 4bit DAC circuit (least significant bit b_0 is not shown) at (a) 100kRads, (b) after being radiated to 175kRads resulting in deterioration through loss of "monotonicity", followed by (c) recovery through Evolution at 175kRads.

TABLE 4: Results with 350kRads.

U1		U2		B1		B2	
Reference	Recovery	Reference	Recovery	Reference	Recovery	Reference	Recovery
IDENTITY							
Failed	Failed	Failed	Recovered	Flat response	Recovery failed	Flat response	Recovery failed
HALF-WAVE RECTIFIER							
Failed	Failed	Output follows the input with very low amplitude	Recovered after 149 generations	Failed	Failed	Failed	Failed
TUNABLE (LOW-PASS) FILTER							
Failed	Failed	Correct		Failed	Failed	Failed	Failed
4 BIT DAC							
Failed	Failed	Failed	Failed	Failed	Failed	Failed	Failed

VI. Conclusions

The paper has presented a mechanism for adapting a mixed analogue reconfigurable platform under total dose radiation faults. Experiments were carried out which exercised the reconfigurable device up to 350Krad radiation dosages demonstrating that the technique is able to recover functionality of blocks such as analogue to digital converters up to 250Krad radiation dosage.

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